

Remarks

The Office Action dated February 16, 2005, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

Claims 7-10 have been amended. The amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 3 and 7-11 are pending in the present application and are respectfully submitted for consideration.

Claims 8, 10 and 11 Rejected under 35 U.S.C. § 103

Claims 8, 10 and 11 were rejected under 35 U.S.C. § 103(a) as being unpatentable over the instant application's disclosed prior art ("AAPA"), specifically figure 1.

As a preliminary matter, Applicants note that the rejection of claims 8, 10 and 11 is unclear since the rejection is based on AAPA, and yet the detailed explanation of the rejection includes a newly referenced art of Wang.

In light of the confusion, Applicants submit that the following remarks for consideration only if the cited prior art is indeed AAPA in view of Wang.

Assuming *arguendo* that claims 8, 10 and 11 were indeed rejected under 35 U.S.C. § 103(a) as being unpatentable over AAPA in view of Wang, then Applicants respectfully traverse the rejection and submit that each of these claims recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 8 recites a delay time adjusting circuit for receiving a signal that is input buffer, as an input signal via the input buffer, and outputting an output signal to an

output buffer, by adjusting a delay time of said input signal comprising, among other features, a dummy circuit configured to delay a signal from said divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

Claim 10 recites a delay time adjusting method for receiving a signal that is input to an input buffer, as an input signal via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal comprising, among other features, the step of delaying the signal obtained by said step (b) by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

In making the rejection, the Office Action characterized Wang as disclosing "a delay adjusting circuit in a phase locking loop shown in figure 5 ... [wherein] a variable delay circuit is disclosed in element 533." The Office Action further acknowledged that "Wang does not disclose using a dummy circuit to delay a signal from the frequency divider by a fixed delay time." The Office Action cited AAPA, Figure 1 in particular, for showing a dummy circuit delaying the signal from the frequency divider.

Applicants submit that Wang in view of AAPA fails to disclose or suggest each and every element recited in claims 8 and 10 of the present application. In particular, claims 8 and 10 recite, in part, that the delay time adjusting circuit receives a signal via an input buffer and outputs a signal via an output buffer, and that a dummy circuit

delays a signal from the divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

As acknowledged by the Examiner, Wang et al. does not teach a dummy circuit to delay an output of the divider by a fixed delay time. Furthermore, the Examiner relies on the AAPA as teaching the dummy circuit, and asserts that it would have been obvious for those skilled in the art to incorporate the dummy circuit of the AAPA into the delay adjusting circuit of Wang et al.

Applicants respectfully disagree and submit that Wang does not teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit. In particular, the “variable delay circuit (element 533)” of Wang is neither comparable nor analogous to the delay time adjusting circuit of the present invention because if the signal output from the buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels. Therefore, Applicants submit that the cited prior art fails to disclose each and every element recited in claims 8 and 10 of the present application.

To establish *prima facie* obviousness, each feature of a rejected claim must be taught or suggested by the applied art of record. See M.P.E.P. §2143.03 and In re Royka, 490 F.2d 981 (CCPA 1974). As explained above, Wang in view of AAPA do not teach or suggest each feature recited in claims 8 and 10. Accordingly, for the above provided reasons, Applicants respectfully submit that claims 8 and 10 are not rendered

obvious under 35 U.S.C. § 103 by the teachings of Wang in view of AAPA, and therefore are allowable.

Under U.S. patent practice, the PTO has the burden under §103 to establish a *prima facie* case of obviousness. In re Fine, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988). Both the case law of the Federal Circuit and the PTO itself have made clear that where a modification must be made to the prior art to reject or invalidate a claim under §103, there must be a showing of proper motivation to do so. The mere fact that a prior art reference could arguably be modified to meet the claim is insufficient to establish obviousness. The PTO can satisfy this burden only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references. Id. In order to establish obviousness, there must be a suggestion or motivation in the reference to do so. See also In re Gordon, 221 USPQ 1125, 1127 (Fed. Cir. 1984) (prior art could not be turned upside down without motivation to do so); In re Rouffet, 149 F.3d 1350 (Fed. Cir. 1998); In re Dembiczak, 175 F.3d 994 (Fed. Cir. 1999); In re Lee, 277 F.3d 1338 (Fed. Cir. 2002). The Office Action restates the advantages of the present invention to justify the combination of references. There is, however, nothing in the applied references to evidence the desirability of these advantages in the disclosed structure.

Applicants respectfully request withdrawal of the rejection.

As claim 11 depends on claim 9, Applicants submit the remarks with respect to claim 11 as provided below.

Claims 3, 7 and 9 Rejected under 35 U.S.C. § 103

Claim 3, 7 and 9 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Wang et al. (U.S. Patent No. 6,448,820, hereinafter "Wang") in view of Hanke, III et al. (U.S. Patent No. 5,376,848, hereinafter "Hanke") further in view of AAPA.

Claim 7 recites a delay time adjusting circuit for receiving a signal that is input to an input buffer, as an input signal via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal comprising, among other features, a dummy circuit configured to delay a signal from said second divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

Claim 9 recites a delay time adjusting method for receiving a signal that is input to an input buffer, as an input signal via the input buffer, and outputting an output signal to an output buffer, by adjusting a delay time of said input signal comprising, among other features, the step of (d) delaying a signal obtained by said step (c) by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

It is respectfully submitted that the prior art fails to disclose or suggest at least the above-mentioned features of the Applicants' invention.

In particular, claims 7 and 9 recites, in part, that the delay time adjusting circuit receives a signal from the second divider by a fixed delay time so as to match phases of the signal input to the input buffer and a signal output from the output buffer.

Wang was discussed above, and fails to teach a dummy circuit. Further, as acknowledged by the examiner, Wang fails to teach two dividers having mutually

different division rates, that is, a second divider having a higher division rate than a first divider which receives the input signal.

Hanke is cited as teaching two dividers having mutually different division rates, but fails to teach or suggest a dummy circuit, and the examiner relies on the AAPA as teaching the dummy circuit that is neither taught in Wang nor Hanke.

Applicants respectfully disagree with the Examiner's position, and submit that neither Wang nor Hanke teach or suggest adjusting a delay time of the input signal so as to match the phases of a signal input to an input buffer that supplies the input signal to the delay adjusting circuit (PLL circuit) and a signal output from an output buffer that outputs an output signal from the PLL circuit. Further, if the signal output from the output buffer were fed back to the PLL circuit via a dummy circuit, the performance of the PLL circuit would deteriorate when the output pattern is not a constant toggle between high and low levels.

For at least the foregoing reasons, Applicants submit that it would not have been obvious for those skilled in the art to incorporate the dummy circuit of the AAPA into the disclosure of Wang and Hanke, and therefore submit that Wang in view of Hanke and further in view of AAPA fail to disclose each and every element recited in claims 7 and 9 of the present application.

As claim 3 depends from claim 7, and claim 11 depends from claim 9, Applicants submit that each of these claims incorporates the patentable aspects therein, and are therefore allowable for at least the reasons set forth above with respect to the independent claims, as well as for the additional subject matter recited therein.

Applicants respectfully request withdrawal of the rejection.

Conclusion

In view of the above, Applicants respectfully submit that each of claims 3 and 7-11 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicants also submit that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 3 and 7-11 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicants respectfully petition for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300.

Respectfully submitted,



Sam Huang
Registration No. 48,430

Customer No. 004372
ARENT FOX PLLC
1050 Connecticut Avenue, N.W.,
Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810